IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1. (Previously Presented) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element provided between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof;

wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of the reactance component of the gate-to-source impedance and said inductor element, and the inductance value of said inductor element is set in accordance with said predetermined frequency of said controlled signal.

Claim 2. (Original) A semiconductor integrated circuit as set forth in claim 1, which further comprises a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

Claim 3. (Currently Amended) A semiconductor integrated circuit as set forth in claim 1, which further comprises a ~~third~~ second capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said ~~third~~ second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

Claim 4. (Original) A semiconductor integrated circuit as set forth in claim 1, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

Claim 5. (Original) A semiconductor integrated circuit as set forth in claim 2, which

Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 8. (Original) A semiconductor integrated circuit as set forth in claim 5, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 9. (Original) A semiconductor integrated circuit as set forth in claim 6, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 10. (Original) A semiconductor integrated circuit as set forth in claim 1, which further comprises a bias supply circuit configured to supply a dc bias voltage to at least one of the gate terminal, drain terminal and source terminal of said FET.

Claim 11. (Previously Presented) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element and a first capacitor element which are connected to each other in series between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a series resonance circuit with a reactance component of a gate-to-source impedance when a drain voltage of said FET is lower than a source voltage thereof;

wherein when a drain voltage of said FET is lower than a source voltage thereof, the series resonance circuit is formed of the reactance component of the gate-to-source impedance and said inductor element, and the inductance value of said inductor element is set in accordance with the predetermined frequency of said controlled signal.

Claim 12. (Original) A semiconductor integrated circuit as set forth in claim 11, which further comprises a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

Claim 13. (Currently Amended) A semiconductor integrated circuit as set forth in claim 11, which further comprises a ~~third~~ second capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said ~~third~~ second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

Claim 14. (Previously Presented) A semiconductor integrated circuit as set forth in claim 11, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and control the magnitude relationship between the drain voltage and the source voltage of said FET.

Claim 15. (Original) A semiconductor integrated circuit as set forth in claim 12, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

Claim 16. (Original) A semiconductor integrated circuit as set forth in claim 13, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

Claim 17. (Original) A semiconductor integrated circuit as set forth in claim 14, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum

Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 19. (Original) A semiconductor integrated circuit as set forth in claim 16, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

Claim 20. (Original) A semiconductor integrated circuit as set forth in claim 11, which further comprises a bias supply circuit configured to supply a dc bias voltage to at least one of the gate terminal, drain terminal and source terminal of said FET.